

PTO/SB/21 - MODIFIED
09/2004

2631

**TRANSMITTAL
FORM***to be used for all correspondence after initial filing*

* plus cited references

Total number of pages in this submission including transmittal

4 *

Application Number

09/737,743

Filing Date

12/18/2000

First Named Inventor

Sehat SUTARDJA

Group Art Unit

2631

Examiner Name

Phuong M. Phu

Attorney Docket Number

MP0020

ENCLOSURES (check all that apply)

- ☐ Fee Transmittal Form
- ☐ Fee Attached - Credit Authorization
- ☐ Amendment / Reply
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement
with PTO 1449 Forms and cited references
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/
Incomplete Application
- ☐ Response to Missing Parts
under 37 CFR 1.52 or 1.53

- ☐ Assignment Papers
(for an Application)
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a
Provisional Application
- ☐ Power of Attorney, Revocation
Change of Correspondence
Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ Landscape Table on CD

- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board
of Appeals and Interferences
- ☐ Appeal Communication to Group
(Appeal Notice, Brief, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (identify below):

REMARKS

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name KATTEN MUCHIN ROSENMAN, LLP

Signature

Printed Name Andrew J. Bateman

Reg. No. 45,573

Date: 08/11/2005

CERTIFICATE OF FACSIMILE TRANSMISSION OR MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO via fax no. (703) 872-9306 or is being deposited with the US Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature

Typed or Printed Name

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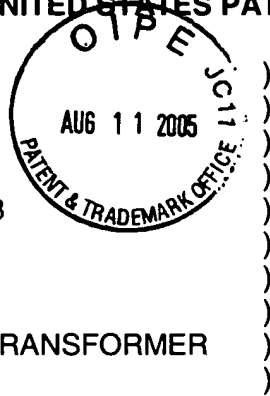
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sehat SUTARDJA, et al.

Application No.: 09/737,743

Filed: December 18, 2000

For: ACTIVE REPLICA TRANSFORMER
HYBRID

Examiner: Phoung M. Phu

Group Art Unit: 2631

Date: August 11, 2005

INFORMATION DISCLOSURE STATEMENTCommissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty of disclosure under 37 CFR § 1.56 and the requirements of M.P.E.P. § 2001.06(c), and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449s and to the attached copies of any non-U.S. Patent or literature references cited thereon.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

No fee is believed necessary for the submission of this Information Disclosure Statement. However, if deemed necessary, the Commissioner is authorized to charge the IDS fee of \$180.00 to Deposit Account No. 50-1710.

Should the Examiner have any questions, Applicant's undersigned attorney is reachable by telephone in our Washington, D.C. office at (202) 625-3547. The correspondence address of record is provided below.

Respectfully submitted,
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FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE		ATTORNEY DOCKET NO. MP0020	APPLICATION NO. 09/737,743
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Sehat SUTARDJA	
		FILING DATE 12/18/2000	GROUP 2631
		DATE SUBMITTED TO USPTO: August 11, 2005	
OTHER DOCUMENTS (Including author, title, date, pertinent pages, etc.)			
*EXAMINER INITIALS			
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	Mano, Digital Logic and Computer Design		
	Farjad-rad, et al., 4.5 A 0.2-2GHz 12mW Multiplying DLL for Low-Jitter Clock Synthesis in Highly Integrated Data Communication Chip		
	Gotoh, et al., All-Digital Multi-Phase Delay Locked Loop for Internal Timing Generation in Embedded and/or High-Speed DRAMS		
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	Sonntag, et al., FAM: 11.5: A Monolithic CMOS 10MHz DPLL for Burse-Mode		
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	Garlepp, et al., A Portable Digital DLL for High-Speed CMOS Interface Circuits		
	Dehng, et al., Clock-Deskaw Buffer Using a SAR-Controlled Delay-Locked Loop		
	Kim, et al., A Low-Power Small-Area 7.28-ps-Jitter 1-GHz DLL-Based Clock Generator		
	Dehng, et al., A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm		
	Lin, et al., A 10-b, 500-Msample/s CMOS DAC in 0.6mm ²		
EXAMINER		DATE CONSIDERED	
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			